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A NOVEL ROBUST ROUTER ARCHITECTURE

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ABSTRACT
The focus of this Paper is the actual implementation of Network Router and verifies the functionality of the three port router for network on chip using the latest verification methodologies, Hardware Verification Languages and EDA tools and qualify the IP for Synthesis an implementation. This Router design contains three output ports and three input ports, it is packet based Protocol. This Design consists Registers and FIFO. For larger networks, where a direct-mapped approach is not feasible due to FPGA resource limitations, a virtualized time-multiplexed approach was used. Compared to the provided software reference implementation, our direct-mapped approach achieves three orders of magnitude speedup, while our virtualized time multiplexed approach achieves one to two orders of magnitude speedup, depending on the network and router configuration.
Keywords :FIFO,Network Router, three port router.

I. INTRODUCTION

90% of ASIC respins are due to functional bugs. As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification/simulation. In order to avoid the delay and meet the TTM, we use the latest verification methodologies and technologies and accelerate the verification process.

This project helps one to understand the complete functional verification process of complex ASICs an SoC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

For most home users, they may want to set-up a LAN (local Area Network) or WLAN (wireless LAN) and connect all computers to the Internet without having to pay a full broadband subscription service to their ISP for each computer on the network.

In many instances, an ISP will allow you to use a router and connect multiple computers to a single Internet connection and pay a nominal fee for each additional computer sharing the connection. This is when home users will want to look at smaller routers, often called broadband routers that enable two or more computers to share an Internet connection. Within a business or organization, you may need to connect multiple computers to the Internet, but also want to connect multiple private networks not all routers are created equal since their job will differ slightly from network to network.

Additionally, you may look at a piece of hardware and not even realize it is a router. What defines a router is not its shape, color, size or manufacturer, but its job function of routing data packets between computers. A cable modem which routes data between your PC and your ISP can be considered a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS, we have a category of hardware routers that are used to perform the same basic task as ICS, albeit with more features and functions. Often called broadband or Internet connection sharing routers, these routers allow you to share one Internet connection to multiple computers.

Broadband or ICS routers will look a bit different depending on the manufacturer or brand, but wired routers are generally a small box-shaped hardware device with ports on the front or back into which you plug each computer, along with a port to plug in your broadband modem. These connection ports allow the router to do its job of routing the data packets between each of the computers and the data going to and from the Internet.

Depending on the type of modem and Internet connection you have, you could also choose a router with phone or fax machine ports.A wired Ethernet broadband router will typically have a

built-in Ethernet switch to allow for expansion. These routers also support NAT (network address translation), which allows all of your computers to share a single IP address on the Internet. Internet connection sharing routers will also provide users with much needed features such as an SPI firewall or serve as DHCP Server.

II. LITERATURE SURVEY

In this we are comparing the existing generic router architecture and our new robust router architecture. This will give the difference in the designing and would reflect our paper enhancements that we are upgrading in our robust router paper.

A. Generic Router Architecture

Channamallikarjuna Mattihalli et al in [1] give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Attempt to provide a multipurpose network-ing router by means of Verilog code, thus we can maintain the same switching speed with more security as we embed the packet storage buffer on chip and generate the code as a self-independent VLSI Based router. The approach will results in increased switching speed of routing per packet for both current trend protocols, which we believe would result in considerable enhancement in networking systems.

Feng Liang et al in [2] proposed a novel test pattern generator (TPG) for built-in self-test. His method generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. A reconfigurable Johnson counter and a scalable SIC counter are developed to generate a class of minimum transition sequences. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. Results show that the produced MSIC sequences have the favorable features of uniform distribution James Aweya et al in [3] give attention to new powerful architectures for routers in order to play that demanding role. In this work, he identified important trends in router design and outlines some design issues facing the next generation of routers. It is also observed that the achievement of high throughput IP routers is possible if the critical tasks are identified and special purpose modules are properly tailored to perform them.

M. Sowmya et al in [4]he attempt is to give a onetime networking solution by the means of merging the VLSI field with the networking field as now a days the router is the key player in networking domain so the focus remains on that itself to get a good control over the network. This paper is based on the hardware coding which will give a great impact on the latency issue as the hardware itself will be designed according to the need.

III. PROPOSED SYSTEM

Given the strict contest deadline and the short implementation window we adopted a set of design principles to spend the available time as efficiently as possible.

This document provides specifications for the Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet.

The router is a" Network Router" has a one input port from which the packet enters. It has three output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 bytes to 63 bytes. Packet header contains three fields DA and length.

Destination address (DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63.

Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data.

The communication on network on chip is carried out by means of router, so for implementing better NOC, the router should be efficiently design. This router supports three parallel connections at the same time. It uses store and forward type of flow control and FSM Controller deterministic routing which improves the performance of router.

The switching mechanism used here is packet switching which is generally used on network on chip. In packet switching the data the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.

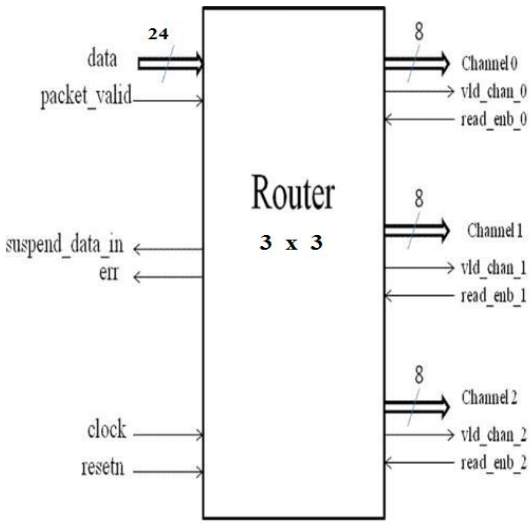


Figure 1- Block Diagram of Three Port Router

FEATURES

- Full duplex synchronous serial data
- Variable length of transfer word up to 64 bytes.
- HEADER is the first data transfer.
- Rx and Tx on both rising or falling edge of serial clock independently
- 3 receivers select
- Fully static synchronous design with one clock domain
- Technology independent
- Fully synthesizable

Router is a Synchronous protocol. The clock signal is provided by the master to provide synchronization. The clock signal controls when data can change and when it is valid for reading.Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data must be timed very accurately.Since ROUTER has a clock signal, the clock can vary without disrupting the data. The data rate will simply change along with the changes in the clock rate.As compared with its counterpart I2C, ROUTER is more suited for data stream applications. Communication between IP's.

OPERATION:

The Three Router Design is done by using of the three blocks .the blocks are 8-Bit Register, Router controller and output block. the router controller is design by using FSM design and the output block consists of three FIFO's combined together the FIFO's are store packet of data and when u want to data that time the data read from the FIFO's. In this router design has three outputs that is 8-Bit size and one 8_bit data port it using to drive the data into router we are using the global clock and reset signals, and the err signal and suspended data signals are output's of the router .the FSM controller gives the err and suspended_data_in signals .This functions are discussed clearly.

The ROUTER can operate with a multiple master device and with one or more slave devices. If a single slave device is used, the RE pin may be fixed to logic low if the slave permits it. Some slaves require the falling edge (high→low transition) of the slave select to initiate an action such as the mobile operators, which starts conversion on said transition. With multiple slave devices, an independent RE signal is required from the master for each slave device.

APPLICATIONS

When multiple routers are used in interconnected networks, the routers exchange information about destination addresses, using a dynamic routing protocol. Each router builds up a table listing the preferred routes between any two systems on the interconnected networks. A router has interfaces for different physical types of network connections, (such as copper cables, fiber optic, or wireless transmission). It also contains firmware for different networking protocol standards. Each network interface uses this specialized computer software to enable data packets to be forwarded from one protocol transmission system to another.

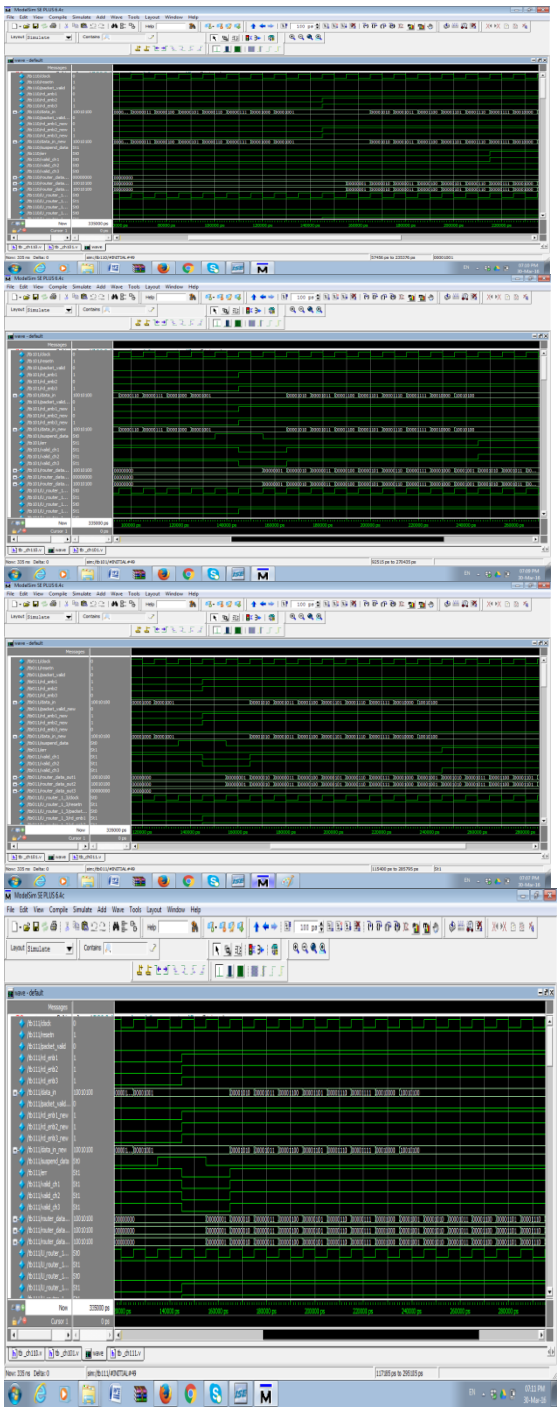
Routers may also be used to connect two or more logical groups of computer devices known as subnets, each with a different sub-network address. The subnets addresses recorded in the router do not necessarily map directly to the physical interface connections.

IV.RESULTS

In this chapter all the simulation results which are done using Xilinx ISE 9.1i are shown and also synthesis results.

A. Simulation Results

Snapshot is nothing but every moment of the application while running. It gives the clear elaborated of application. It will be useful for the new user to understand for the future steps.



V. CONCLUSION

In this router project verified the functionality of router with the latest Design methodology i.e., Verilog and observed the code coverage and functional coverage of router by using cover points,cross and different test cases(like constrained, weighted and directed test cases). By using these test cases improved the functional coverage of router. In this we used three masters and three slaves to monitor the router. Thus the constraints coverage of router was improved by reducing the usage of no of LUTs and memory utilize requirements by improving the frequency.Finally we will design the proposed structure using Verilog HDL Language and simulated by using Modelsim 6.4c and synthesized using Xilinx 9.1

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